In the specification

Please replace the paragraph on page 10, lines 8-18, with the following paragraph.

A.) This part covers in further detail the construction of the effector machines in the initial population. Each machine is constructed separately. The structure of how connections and effectors are organized in a machine must be explained first. Each machine that is designed by cyclic graph evolution is composed of one Input module, one Output module, and one or more Internal modules. ~~(~~Refer to the ~~diagram~~ Figure 1 titled *Effector Machine Structure used in Cyclic Graph Evolution.*~~)~~ In Figure 1, internal connections lie completely within one rectangle, which represents one module. Non-zero external connections run from one module to another module. Effectors that have non-zero external connections to other modules are shown as large dots. Although a module may contain multiple effectors, ~~E~~every effector lies in exactly one module. This structure does not affect how the Effector machine computes, as explained in Section 2, but it does affect how two machines are created for CGE, crossed over and mutated. A non-zero connection between two effectors lying in two distinct modules is called an *external connection.* A non-zero connection between two effectors lying in the same-module is called an *internal connection.*

Please replace the paragraph on page 11, lines 3-10, with the following paragraph.

B.) This part explains how CGE executes a crossover between two machines, machine A and machine B. Please refer to the ~~diagram~~ Figure 2 titled, *CGE Crossover.* The variable n_1 represents the number of internal modules in the machine A, and n_2 represents the number of internal modules in machine B. For machine A, a random whole

number j_1 is chosen, lying between LOWER FRACTION NUM MODULES * n_1 and UPPER FRACTION NUM MODULES * n_1. For machine B, a random whole number j_2 is chosen, lying between LOWER FRACTION NUM MODULES * n_2 and UPPER FRACTION NUM MODULES * n_2.

Please replace the paragraph on page 11, lines 11-20, with the following paragraph.

In the ~~diagram~~Figure 2, for machine A, $j_1 = 2$ was selected. For machine B, $j_2 = 1$ was selected. Since $j_1 = 2$, two distinct numbers are chosen randomly from the set $\{1, 2, \ldots . n_1\}$. For machine A, these two numbers are 2 and 3. Since $j_2 = 1$, one number is randomly chosen from $\{1, 2, \ldots . n_2\}$. In this case, 2 was chosen. What all this means is that internal modules m_2 and m_3 of Machine A are crossed over with internal module m_2' of Machine B. All the external connections to these modules are also severed. In the diagram, after crossover, new external connections are created and added to the internal modules that were crossed over. Observe that internal connections in a module that is crossed over are not changed or severed after crossover. This is why these objects are called modules. Internal connections are not severed by a crossover.

Please replace the paragraph on page 12, lines 8-11, with the following paragraph.

In a directed graph diagram, a dot represents a vertex. A line segment with one arrow pointing from one vertex to the other vertex represents a directed edge. The ~~diagram~~ Figure 3 titled, *Directed Graphs* shows one graph that contains a cycle and another that does not contain a cycle so it is called a tree.

Please replace the paragraph on page 13, lines 15-23, with the following paragraph.

Let r denote the refractory period of an effector. Let t_{detect} denote the time at which effector E_i detects some other effector fired. Let t_{actual} denote the actual time that this other effector fired. To make the analysis simpler to present, we ignore the transmission time from the effector that fired to the effector that received this firing information. Let ϵ_i denote the maximum possible value for $|t_{detect} - t_{actual}|$. Define $\epsilon = \max\{\epsilon_i : E_i$ *is an effector in machine* M$\}$. If $\epsilon = 0$, then all effectors detect when another effector has fired with perfect precision. Let T denote a finite interval of time such that the hardware obeys $0 \leq \epsilon < r < T$. Refer to the ~~diagram~~Figure 4, titled *Error Tolerance in Effectors*.

Please replace the paragraph bridging pages 13 and 14 with the following paragraph.

The schematic ~~diagram~~ Figure 5 titled *Effector Circuit* illustrates how one Effector can be implemented with a circuit built from transistors that operate subthreshold. This technique reduces the amount of power consumed by more than 5 orders of magnitude. In Carver Mead's words, for a transistor to operate subthreshold means: " The gate voltage at which the mobile charge [in the transistor] begins to limit the flow of current is called the threshold voltage .... Most circuits described in this book operate in subthreshold – their gate voltages are well below the threshold voltage," [MEAD]. Furthermore, when transistors operate subthreshold, the amount of heat produced is greatly reduced.